

CLAIMS:

1. Arrangement on a semiconductor chip for calibrating a temperature setting curve having
 - a signal generation unit (2) for providing a first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}), which is proportional to the actual temperature T_1 of the chip, whereby a
 - 5 signal offset (I_{virt} , V_{virt} , f_{virt}) is creatable by the signal generation unit (2), which is combined with the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) defining a second signal (I_{ptat2} , V_{ptat2} , f_{ptat2});
 - a signal extraction unit (3) receiving the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) and the second signal (I_{ptat2} , V_{ptat2} , f_{ptat2}) for calculating a first temperature
 - 10 point (T_1) based on the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) and a second temperature point (T_2) based on the second signal (I_{ptat2} , V_{ptat2} , f_{ptat2}).
2. Arrangement as claimed in claim 1, whereby the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}), which is proportional to the actual temperature (T_1) of the chip, is a current (I_{ptat1}),
 - 15 a voltage (V_{ptat1}) or a frequency (f_{ptat1}).
3. Arrangement as claimed in claim 1, whereby the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) and the second signal (I_{ptat2} , V_{ptat2} , f_{ptat2}) are convertible into digital signals, whereby the temperature extraction unit (3) calculates the first and second temperature
 - 20 points (T_1 , T_2) for calibrating the temperature setting curve.
4. Method for calibrating a temperature setting curve of a temperature sensor arrangement on a semiconductor chip, the method comprising:
 - reading a first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}), which is proportional to
 - 25 the actual temperature (T_1) of the chip

- generating a signal offset (I_{virt} , V_{virt} , f_{virt}), which is combined with the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) defining a second signal (I_{ptat2} , V_{ptat2} , f_{ptat2})
- extracting a first actual temperature T_1 from the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) and a second temperature (T_2) from the second signal (I_{ptat2} , V_{ptat2} , f_{ptat2})

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5. Method as claimed in claim 4, whereby the resulting temperatures (T_1 , T_2) are used for providing calibration parameters to the chip.
 6. Method as claimed in claim 5, whereby calculating calibration parameters can be performed on-chip or off-chip.
 7. Method as claimed in claim 4, whereby additional signal offsets (I_{virt2} , V_{virt2} , f_{virt2}) are provided for calculating more than two temperature points (T_n) and calibrating a non linear temperature setting curve.
 8. Method as claimed in claim 4, whereby the signal offset (I_{virt} , V_{virt} , f_{virt}) is subtracted from first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) or added to the first signal (I_{ptat1} , V_{ptat1} , f_{ptat1}) defining the second signal (I_{ptat2} , V_{ptat2} , f_{ptat2}), which is provided to the temperature extraction unit (3).